



H61H2-M5

Rev :2.0

ECS CONFIDENTIAL

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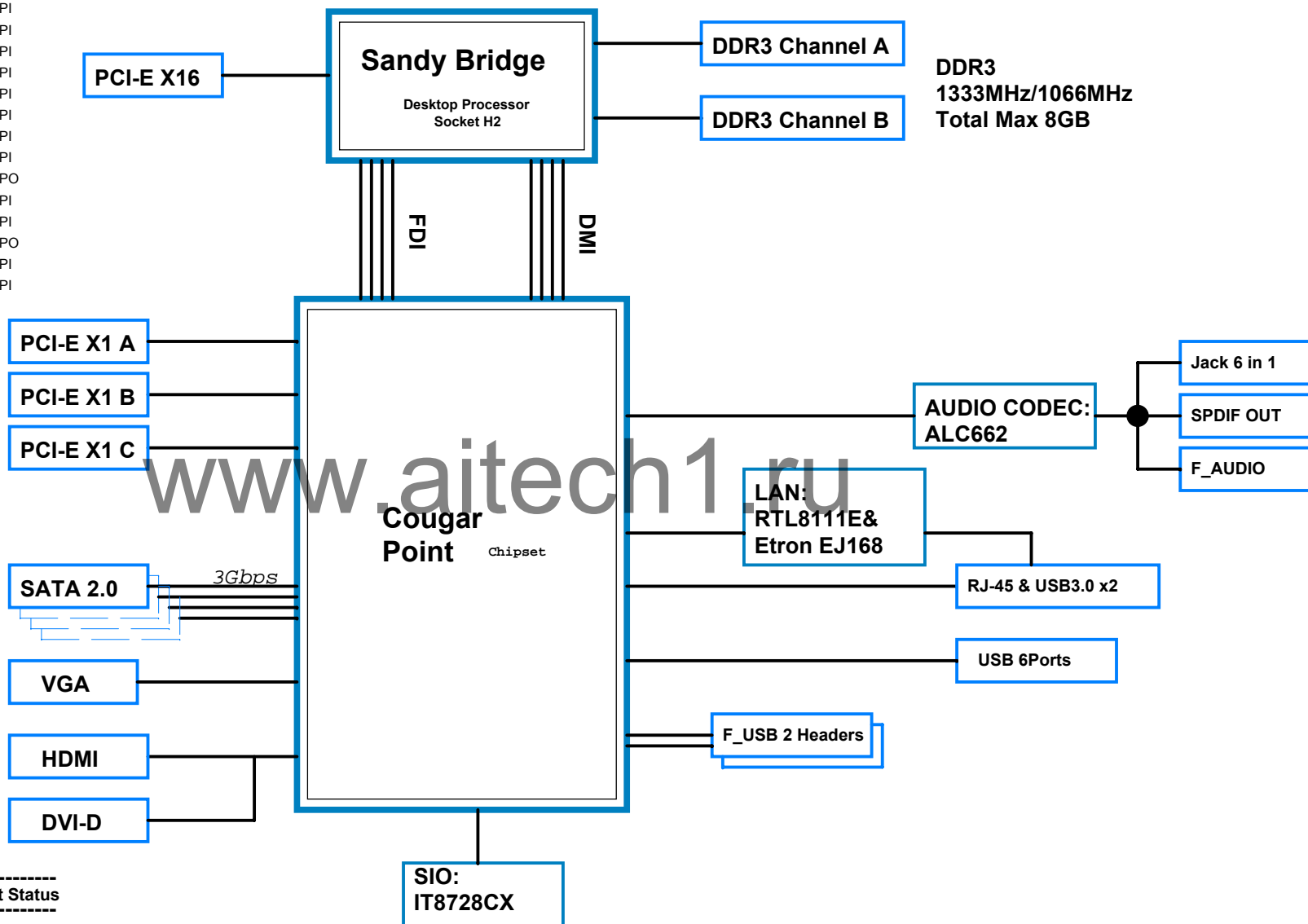
NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

REVISION HISTORY:

| Rev | Date | Notes |
|-------|------------|---|
| V.A | 2010/11/09 | Change from H67H2-M3: 1. Del PCI SLOT *2&Add PCIEx1 slot *2 2. Del PCI Bridge IT8893CX 3. Add TPM/LPT/LPC DEBUG HEADER 4. Super IO change to IT8728CX 5. Chipset change to H61 |
| V.1.0 | 2010/12/06 | Change from H61H2-M5:VA 1.P23 change 5V_CTRL FOR EZ_CHANGE 2.P24 CHANGE Cg FOR COLAY VIA 1705CE 2010/12/06 FQ 3.P23 ADD VIN2 VIN5 VIN6 20101208 ADD FOR RESERVE 2010/12/09 4.P25 change front line damping resistor 75ohm to 16ohm when in stall VIA codec 5. P13 Add 4PIN SYSFAN2 1211 FQ Change 12V EC, MC110/MC111 10U-16VY-12 6. P22 Change SATA1/2 footprint 90度 7. P23 PCH_THRM_L NO connect ,PULL HIGH VCC3 8. P28 USB3 USE NEC720200 9. P9/P10 PWM RT8859MGQW + RT9612BGS SUS RT8859AGQW + RT9619APS 10.P21/22 Change USBX4 TO USBX2 , PS2 Change TO PSUSB 1213 11.P13 CHANGE 4PIN SYS&PWR FAN TO 3PIN FAN |
| V.2.0 | 2011/01/18 | Change from H61H2-M5 V 1.0: 1. Del HDMI CONNECT (P21) 2. DEL LPT HEADER, 3. change P23 I/O BC230 TO 1U-06 ,ADD P13 C70,C71 4. Change Audio chip to ALC892 COY-LAY ALC662 |

PCH-GPIO function

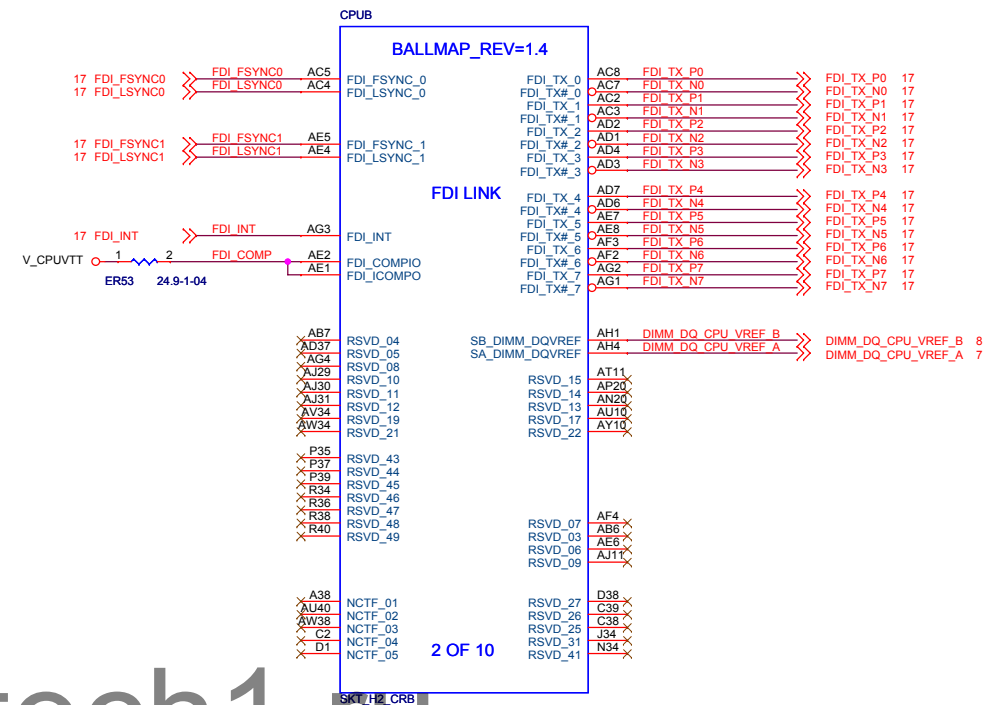
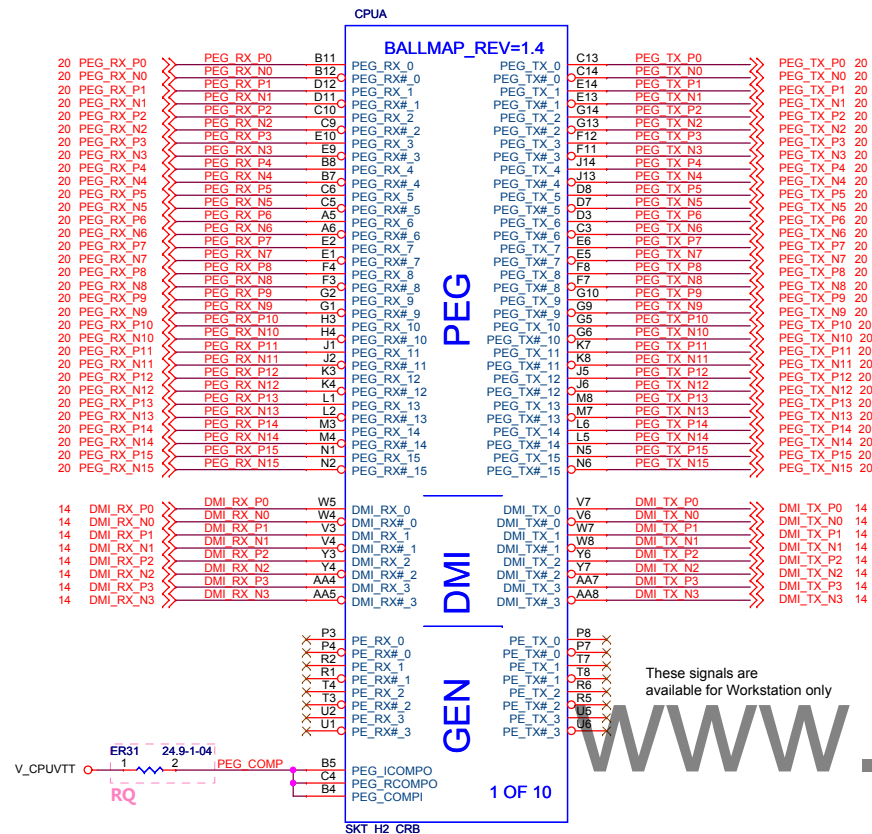
| Pin Name | Power Well | Usage | Default Status |
|----------|------------|-------------------|----------------|
| GPIO71 | VCC3 | | GPI |
| GPIO22 | VCC3 | | GPI |
| GPIO38 | VCC3 | | GPI |
| GPIO39 | VCC3 | | GPI |
| GPIO48 | VCC3 | | GPI |
| GPIO21 | VCC3 | | GPI |
| GPIO36 | VCC3 | | GPI |
| GPIO37 | VCC3 | | GPI |
| GPIO16 | VCC3 | Reserve for TPM | GPI |
| GPIO49 | VCC3 | Reserve for TPM | GPI |
| GPIO0 | VCC3 | F_AUDIO Detect | GPI |
| GPIO33 | VCC3 | ME Enable/Disable | GPO |
| GPIO34 | VCC3 | pull-up | GPI |
| GPIO13 | 3VSB | PME | GPI |
| GPIO24 | 3VSB | SKTOCC | GPO |
| GPIO57 | 3VSB | Board ID(CRB_0.7) | GPI |
| GPIO61 | 3VSB | TPM_LPCPD | GPI |



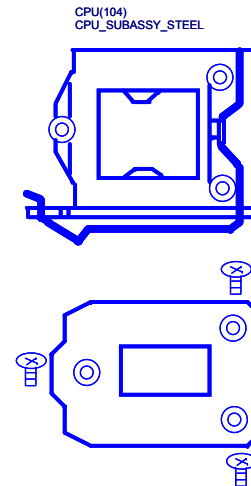
DDR3
1333MHz/1066MHz
Total Max 8GB

SIO-GPIO function

| Pin Name | Power Well | Usage | Default Status |
|----------|------------|-----------|----------------|
| GP16 | VCC3 | BEEP | |
| GP23 | | Power LED | |
| GP22 | | Power LED | |
| Pin Name | | Usage | |
| Pin Name | | Usage | |
| Pin Name | | Usage | |
| Pin Name | | Usage | |



SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
 1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.



11-018-115021 CPU SMD SOCKET
 SOCKET.CPU.LGA 1155P SMD BLACK,PE115527-4041-01F.
 LEAD-FREE.FOXCONN

20-800-004711 CPU SOCKET STEEL
 SUBASSY.STEEL LGA 1155P-W/
 BACK PLATE.PT44A11-6401-LEAD-FREE(RoHS).FOXCONN

01D201-000060 PCH ES0

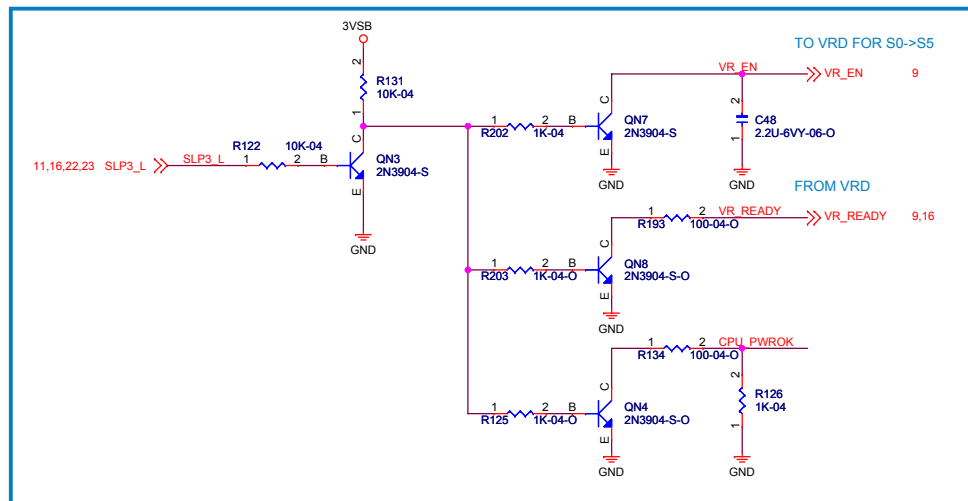
| CFG | H | L | DESCRIPTION |
|-----|----------|----------|--------------------------|
| 0 | reserved | reserved | reserved |
| 1 | reserved | reserved | reserved |
| 2 | NORMAL | REVERSE | PEGLANE REVERSAL[0], X16 |
| 3 | reserved | reserved | reserved |
| 4 | reserved | reserved | reserved |
| 5 | * | * | PEOFSEL[0] |
| 6 | * | * | PEOFSEL[1] |
| 7 | reserved | reserved | reserved |
| 8 | reserved | reserved | reserved |
| 9 | reserved | reserved | reserved |
| 10 | reserved | reserved | reserved |
| 11 | reserved | reserved | reserved |
| 12 | reserved | reserved | reserved |
| 13 | reserved | reserved | reserved |
| 14 | reserved | reserved | reserved |
| 15 | reserved | reserved | reserved |

CFG[0..17] HAVE INTERNAL PULL-UPS

| PCIE CONFIG | SEL0 | SEL1 |
|-------------|------|------|
| 1 X 16 | 1 | 1 |
| 2 X 8 | 0 | 1 |

CFG[5:6]:
 11=DEFAULT X16,
 01=X2X8,
 10=RESERVED,
 00=X8,X4,X4

Power Down Sequencing Circuit

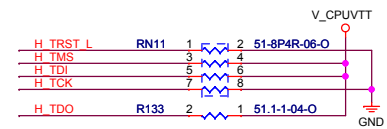
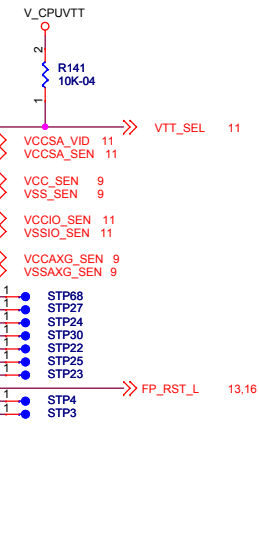


change test point for internal PU Jack05/25

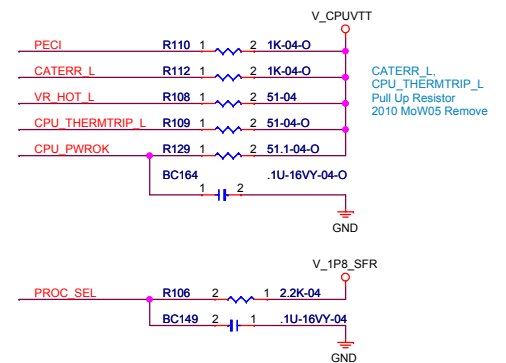
www.aitech1.com

5 OF 10

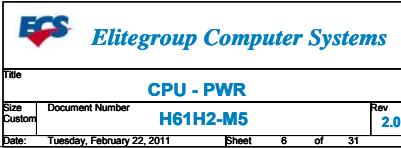
SKT_H2_CRB



EDS P68/132 has internal PU Jack05/25

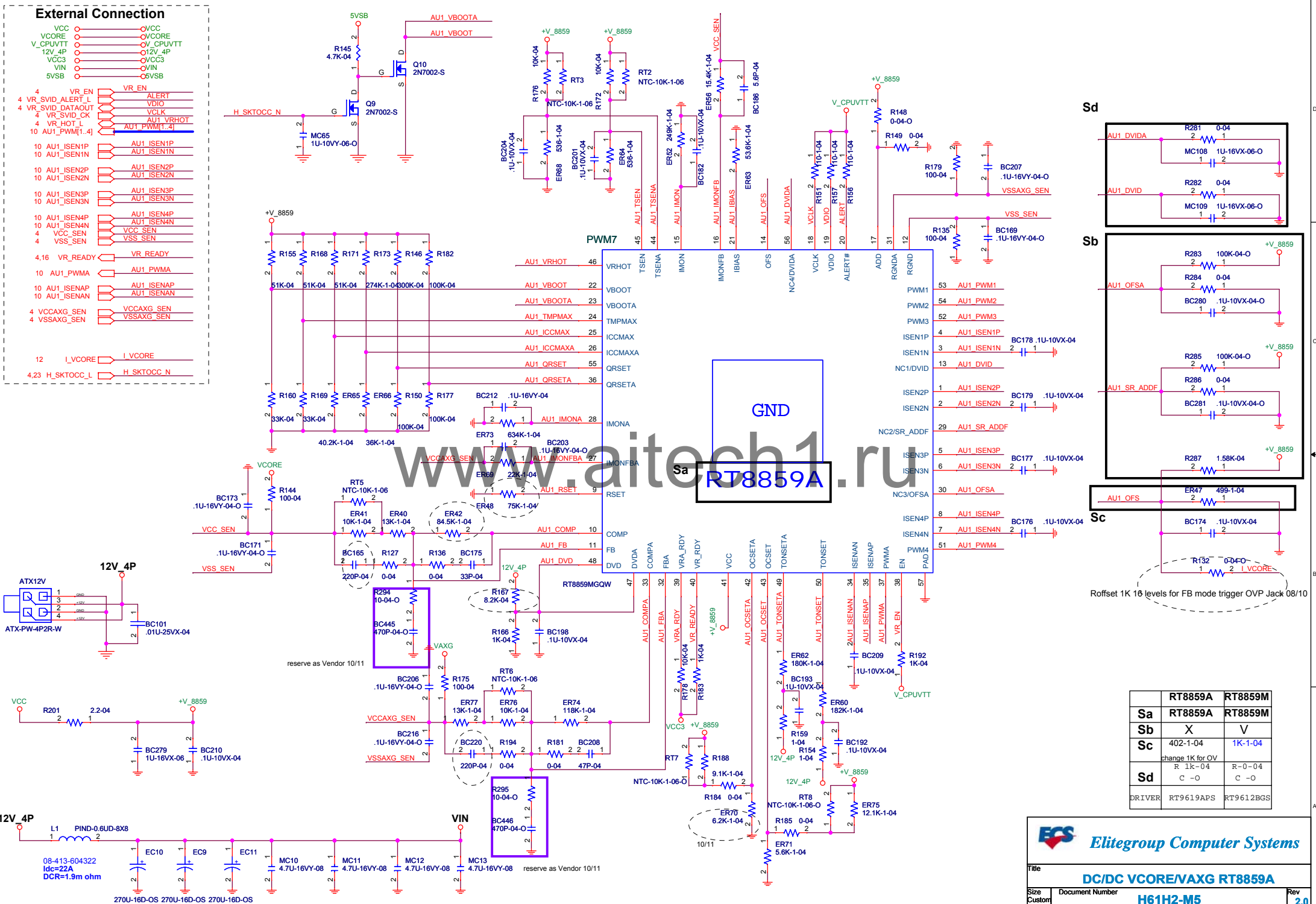


DMI/FDI termination voltage:
 DC coupled: TX/RX to VCC ISF sampled high
 DC coupled: TX/RX TO VSS IF sampled low
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap



External Connection

| Pin | Signal | Pin | Signal |
|-----------------|----------------|-----------------|----------------|
| VCC | VCC | VCC | VCC |
| VCCORE | VCCORE | VCCORE | VCCORE |
| V_CPUVTT | V_CPUVTT | V_CPUVTT | V_CPUVTT |
| 12V_4P | 12V_4P | 12V_4P | 12V_4P |
| VCC3 | VCC3 | VCC3 | VCC3 |
| VIN | VIN | VIN | VIN |
| 5VSB | 5VSB | 5VSB | 5VSB |
| VR_EN | VR_EN | VR_EN | VR_EN |
| VR_SVID_ALERT_L | ALERT | VR_SVID_ALERT_L | ALERT |
| VR_SVID_ALERT_U | VDDIO | VR_SVID_ALERT_U | VDDIO |
| VR_SVID_CLK | VLCK | VR_SVID_CLK | VLCK |
| VR_HOT_L | AU1_VRHOT | VR_HOT_L | AU1_VRHOT |
| AU1_PWM1[1..4] | AU1_PWM1[1..4] | AU1_PWM1[1..4] | AU1_PWM1[1..4] |
| AU1_ISEN1P | AU1_ISEN1P | AU1_ISEN1P | AU1_ISEN1P |
| AU1_ISEN1N | AU1_ISEN1N | AU1_ISEN1N | AU1_ISEN1N |
| AU1_ISEN2P | AU1_ISEN2P | AU1_ISEN2P | AU1_ISEN2P |
| AU1_ISEN2N | AU1_ISEN2N | AU1_ISEN2N | AU1_ISEN2N |
| AU1_ISEN3P | AU1_ISEN3P | AU1_ISEN3P | AU1_ISEN3P |
| AU1_ISEN3N | AU1_ISEN3N | AU1_ISEN3N | AU1_ISEN3N |
| AU1_ISEN4P | AU1_ISEN4P | AU1_ISEN4P | AU1_ISEN4P |
| AU1_ISEN4N | AU1_ISEN4N | AU1_ISEN4N | AU1_ISEN4N |
| VCC_SEN | VCC_SEN | VCC_SEN | VCC_SEN |
| VSS_SEN | VSS_SEN | VSS_SEN | VSS_SEN |
| VR_READY | VR_READY | VR_READY | VR_READY |
| AU1_PWMMA | AU1_PWMMA | AU1_PWMMA | AU1_PWMMA |
| AU1_ISENAP | AU1_ISENAP | AU1_ISENAP | AU1_ISENAP |
| AU1_ISENAN | AU1_ISENAN | AU1_ISENAN | AU1_ISENAN |
| VCCAGX_SEN | VCCAGX_SEN | VCCAGX_SEN | VCCAGX_SEN |
| VSSAGX_SEN | VSSAGX_SEN | VSSAGX_SEN | VSSAGX_SEN |
| I_VCORE | I_VCORE | I_VCORE | I_VCORE |
| H_SKTOCC_L | H_SKTOCC_N | H_SKTOCC_L | H_SKTOCC_N |



| | | |
|-----------|------------------------------|----------------|
| | RT8859A | RT8859M |
| Sa | RT8859A | RT8859M |
| Sb | X | V |
| Sc | 402-1-04 change 1K for OV | 1K-1-04 |
| Sd | R 1k-04 C -O | R-0-04 C -O |
| DRIVER | RT9619APS | RT9612BGS |

External Connection

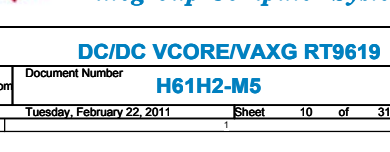
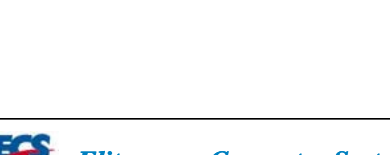
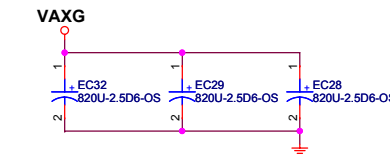
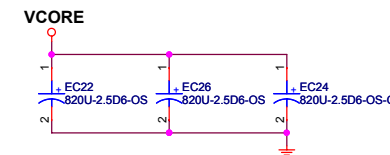
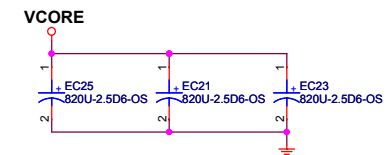
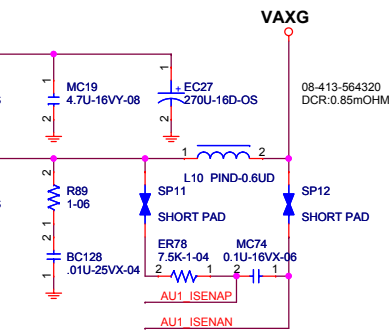
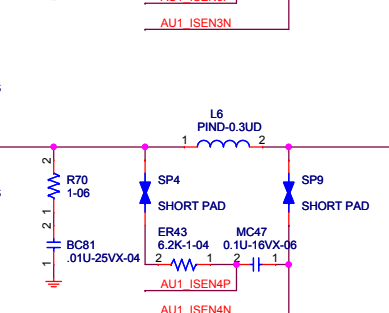
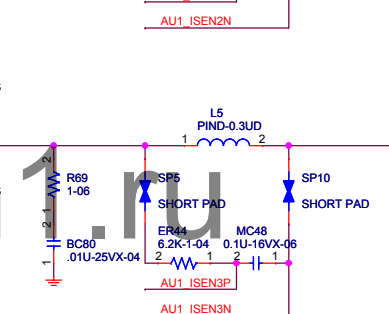
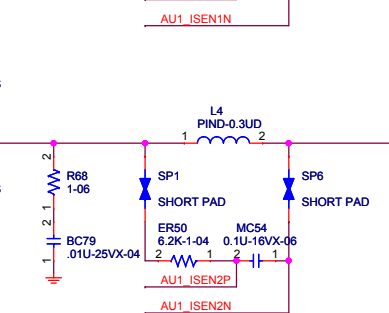
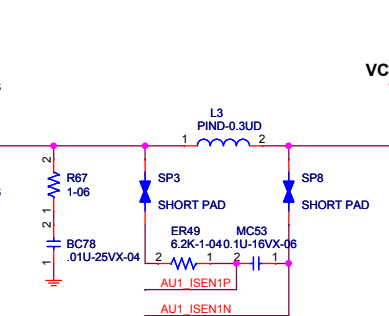
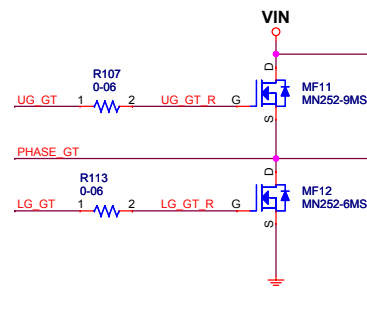
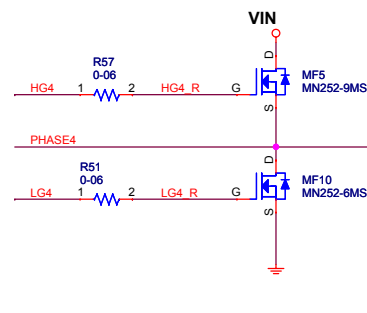
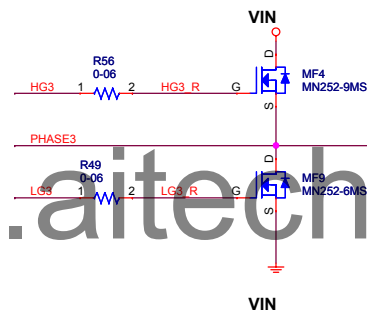
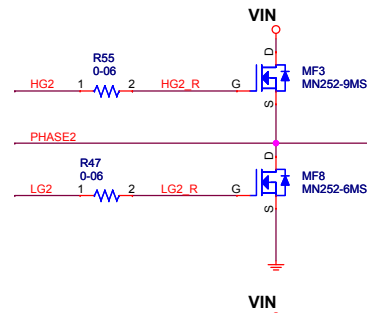
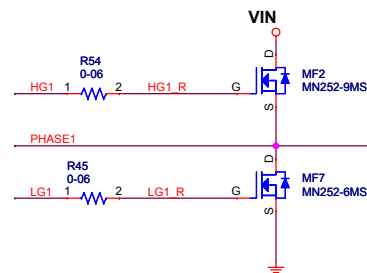
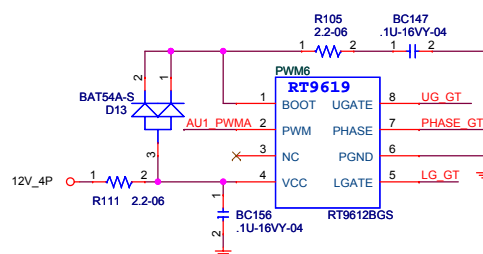
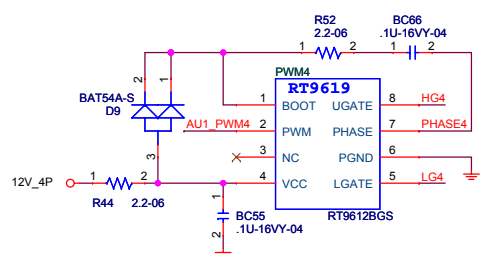
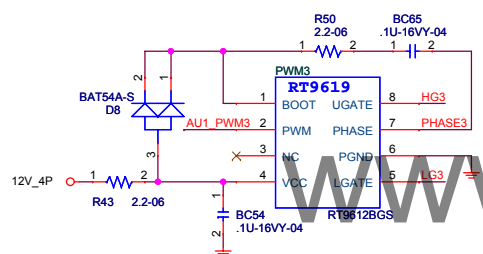
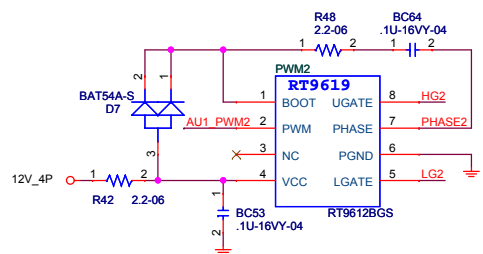
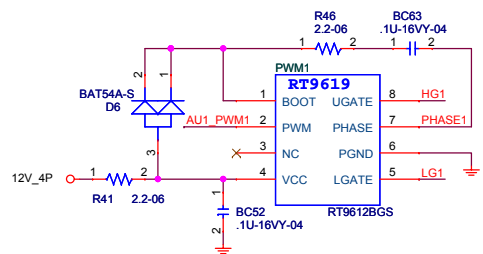
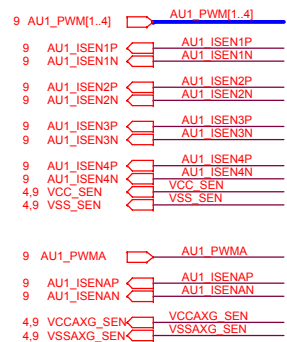
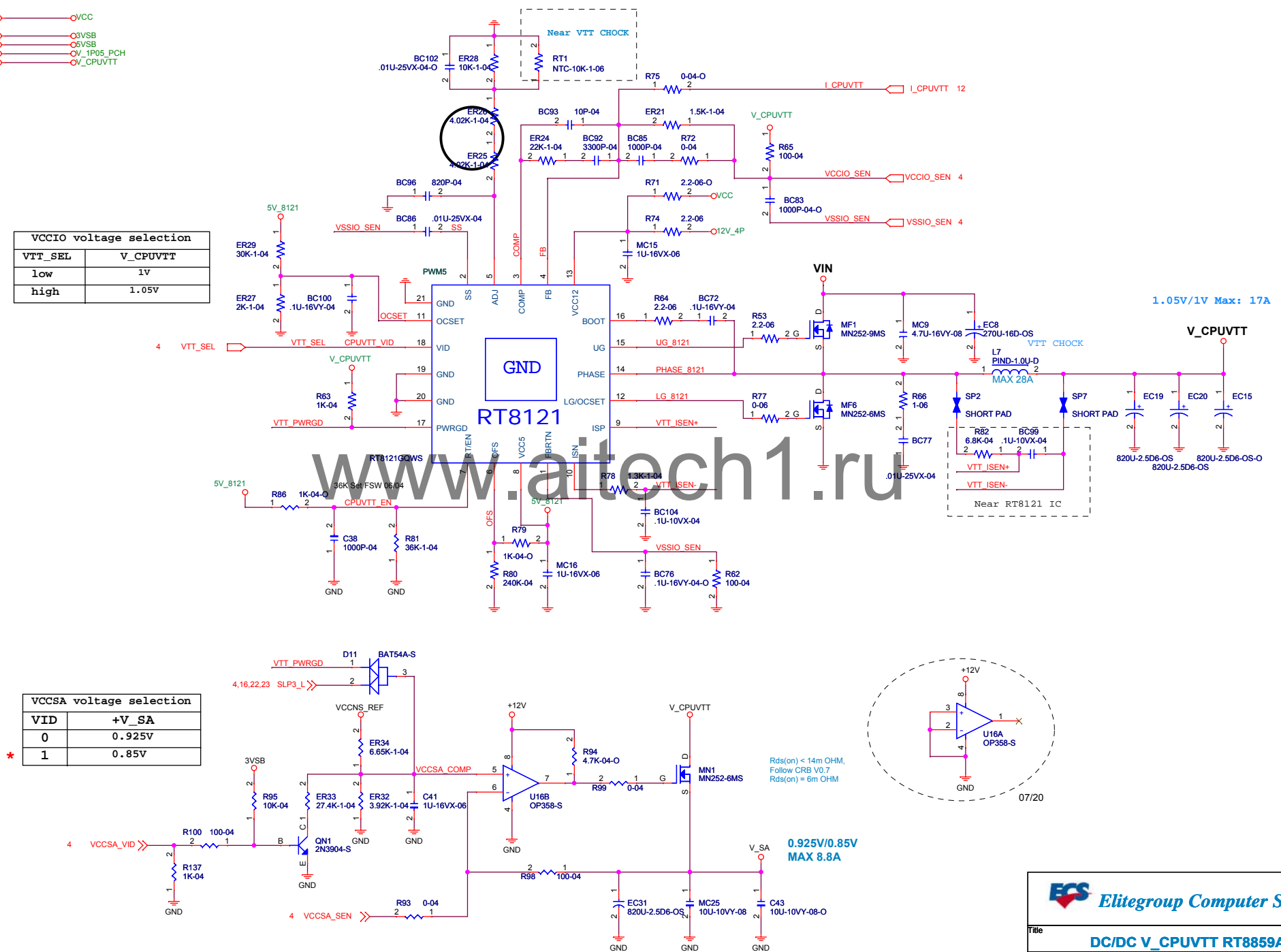


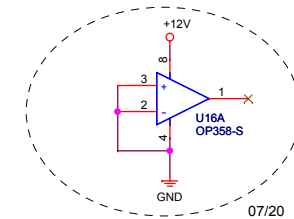
Diagram illustrating the pin-to-pin connections for the module:

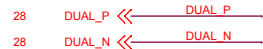
- VCC is connected to VCC.
- 3VSB is connected to 3VSB.
- 5VSB is connected to 5VSB.
- V_1P05_PCH is connected to V_1P05_PCH.
- V_CPUVTT is connected to V_CPUVTT.

| VCCIO voltage selection | |
|-------------------------|----------|
| VTT_SEL | V_CPUVTT |
| low | 1V |
| high | 1.05V |

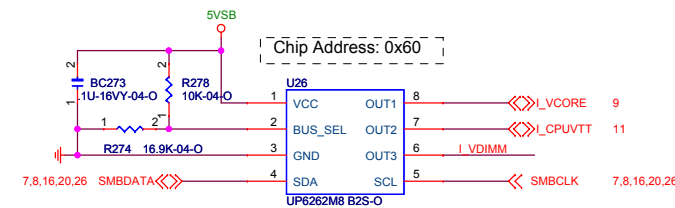
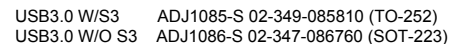
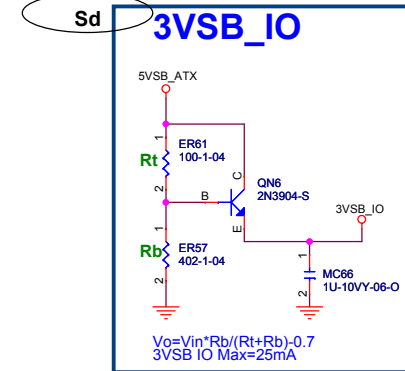
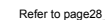
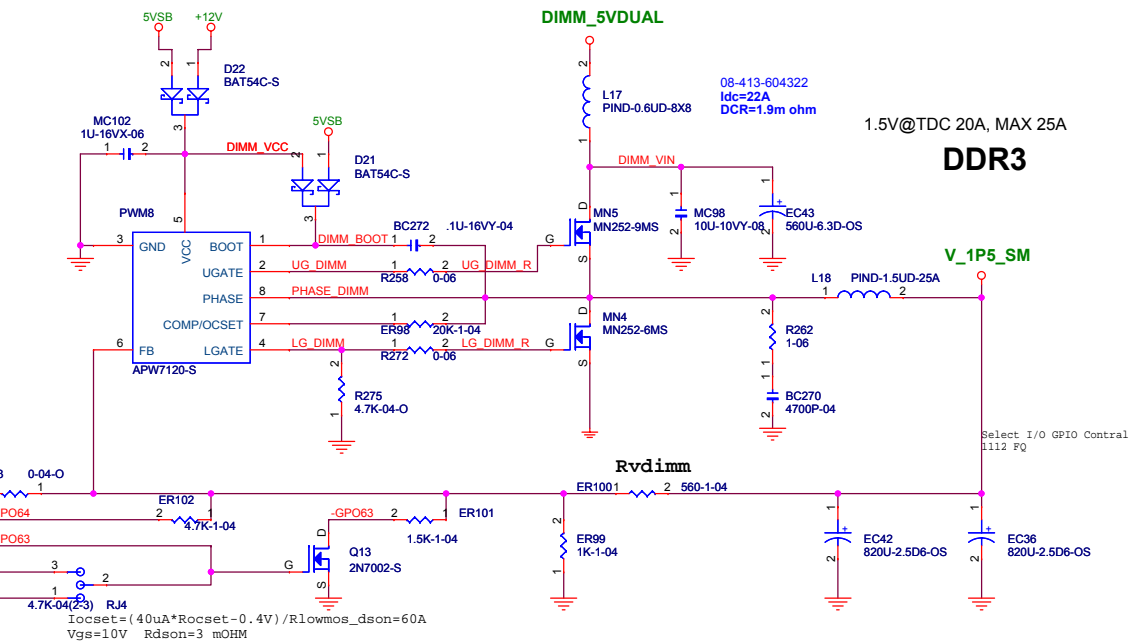


| VCCSA voltage selection | |
|-------------------------|--------|
| VID | +V_SA |
| 0 | 0.925V |
| 1 | 0.85V |

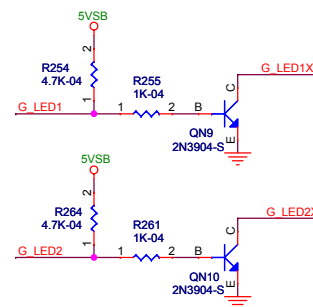
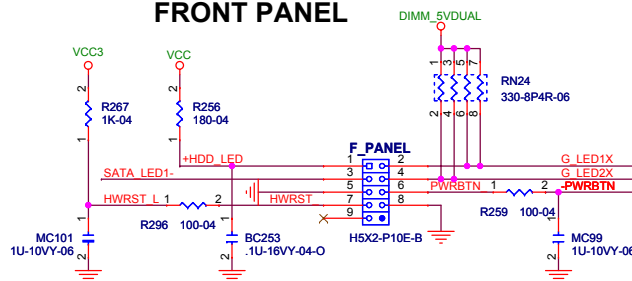
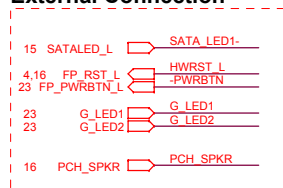




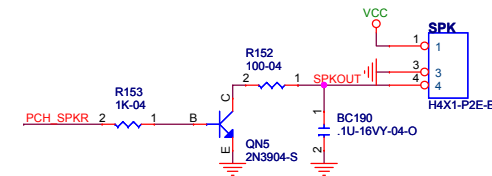
| | | |
|--------|-------|-------|
| -GP063 | GP064 | VDIMM |
| 1 | 1 | 1.25V |
| 1 | 0 | 1.35V |
| 0 | 1 | 1.55V |
| 0 | 0 | 1.65V |



FRONT PANEL

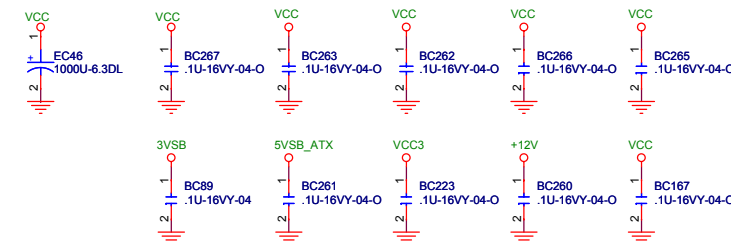
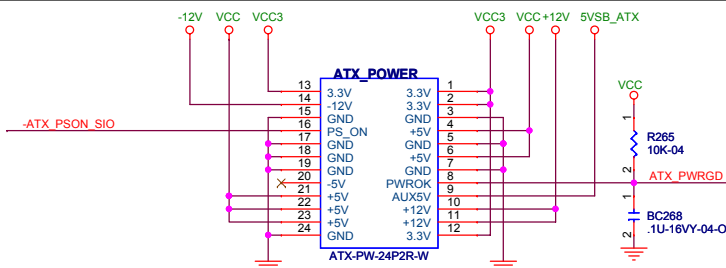
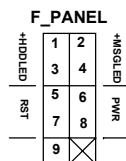
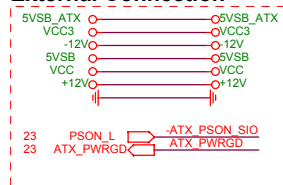


| | | | | | |
|--------|----|----|----|-----|----|
| | S0 | S1 | S3 | S4 | S5 |
| G LED1 | L | B | B | L | |
| G LED2 | H | H | L | L | |
| | G | GB | YB | OFF | C |



POWER CONNECTOR

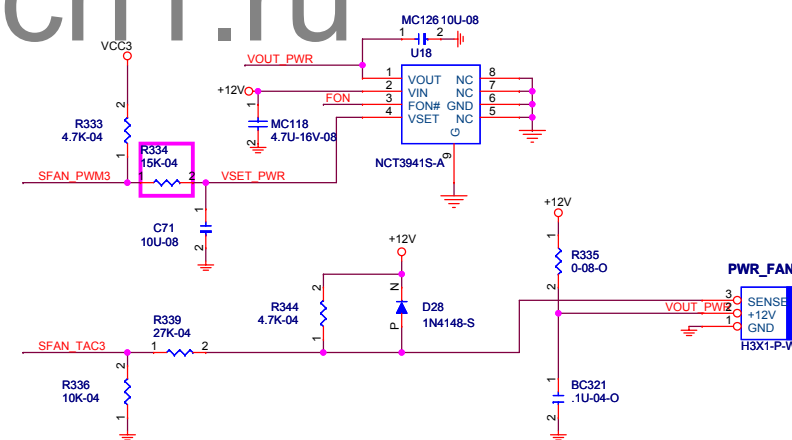
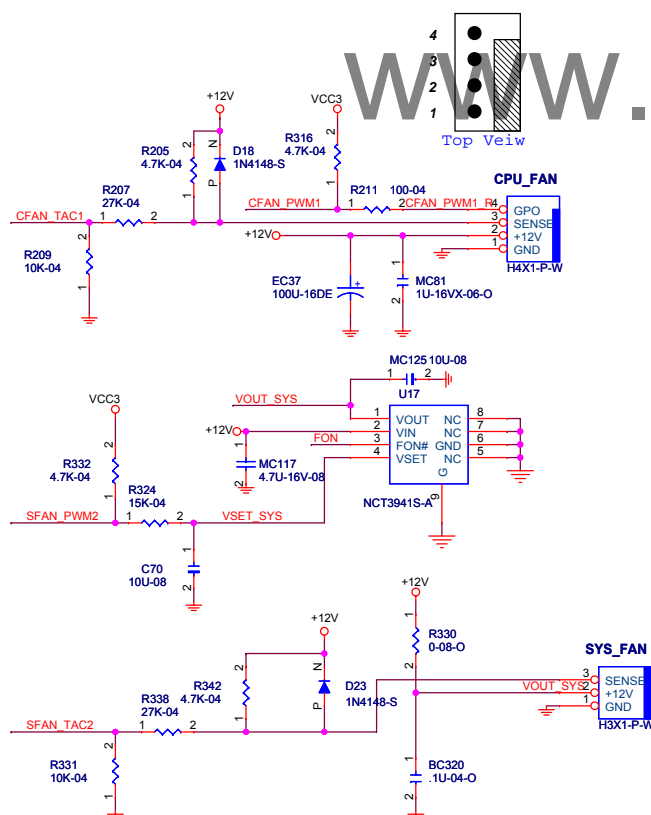
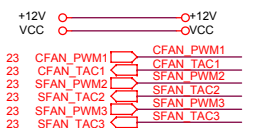
External Connection



For EMI.

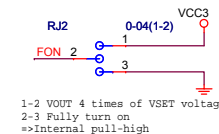
FAN

External Connection



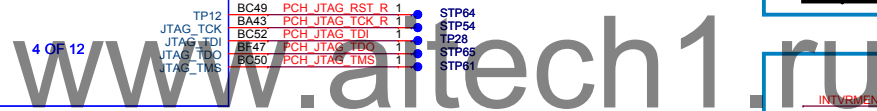
FQ 1217

Add 3 pin control Fan

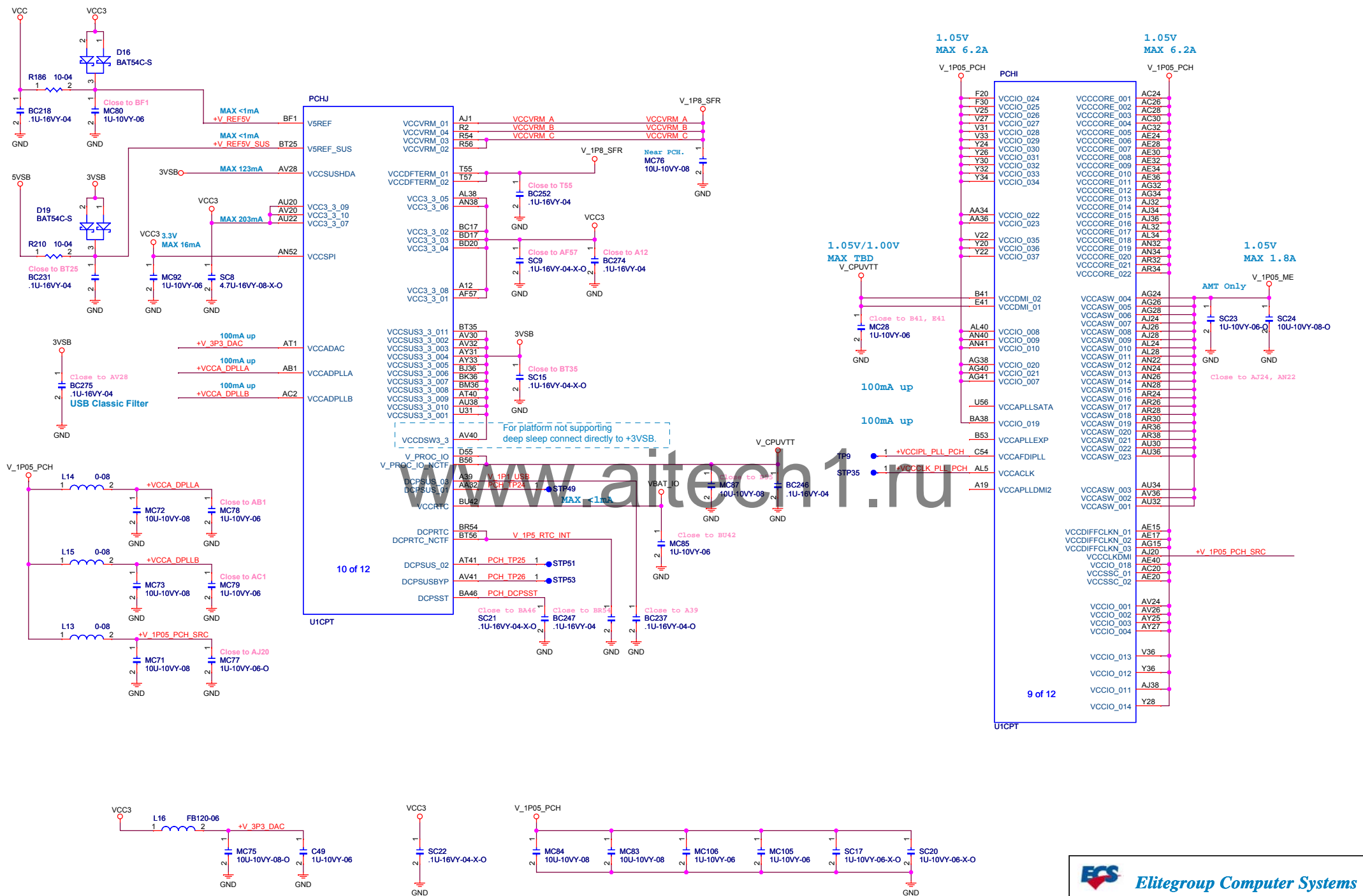


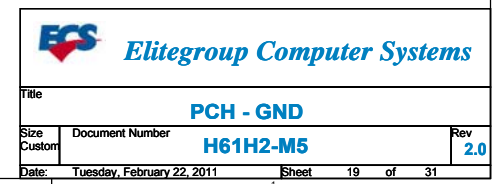
Elitegroup Computer Systems

| | | | |
|---------------------------|------------------------------|----------------|--------|
| Title | | | |
| Front Panel,FAN,PowerConn | | | |
| Size Custom | Document Number | H61H2-M5 | Rev 2. |
| Date: | Wednesday, February 23, 2011 | Sheet 13 of 31 | |

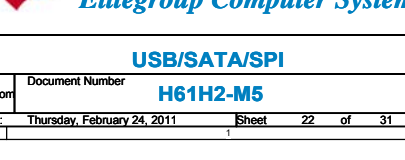
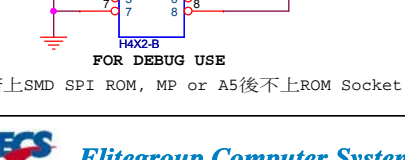
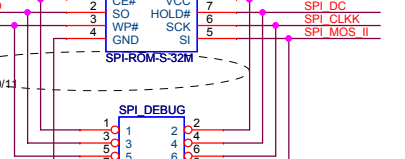
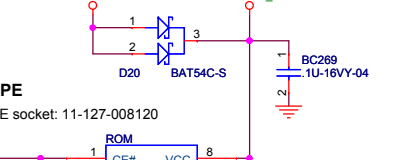
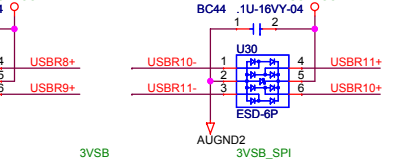
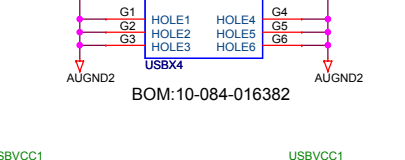
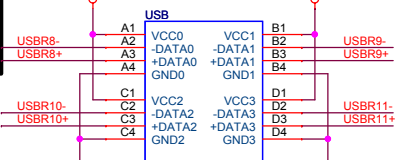
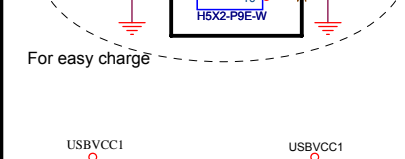
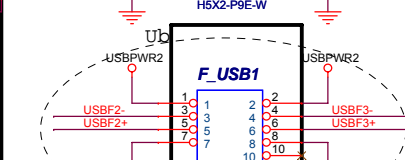
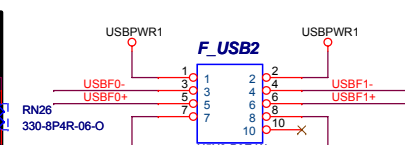
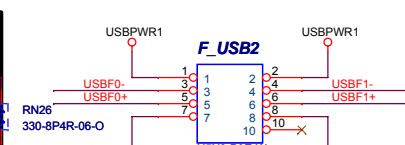



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| Rev | 2.0 |
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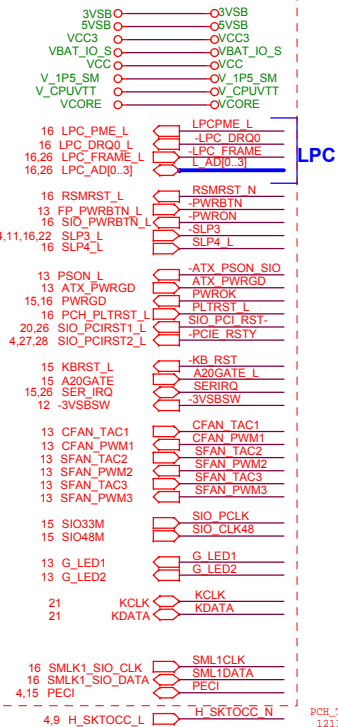




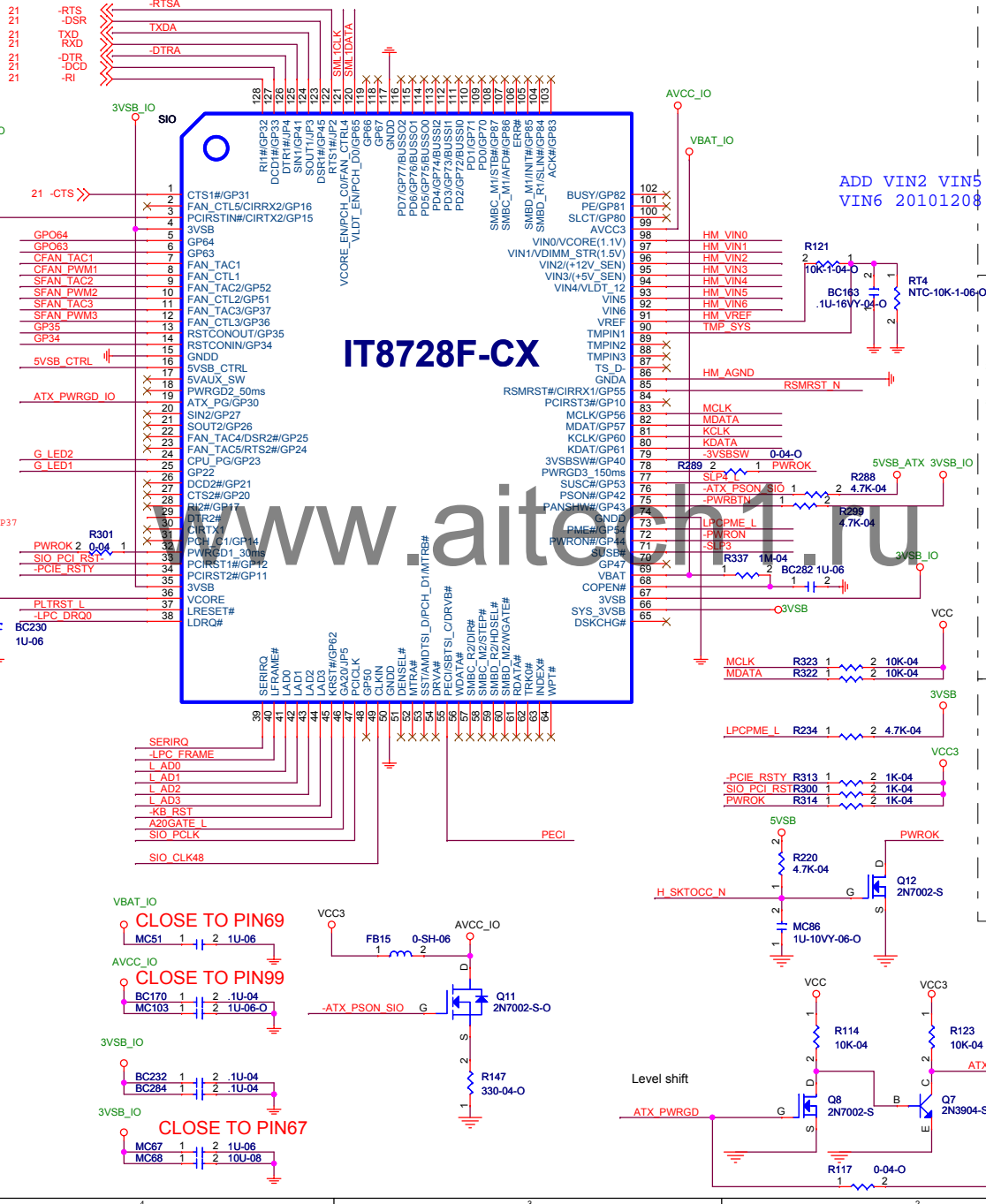
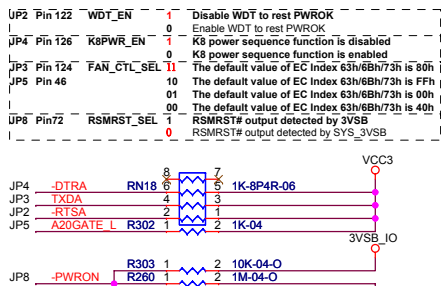


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|  Elitegroup Computer Systems | |
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| USB/SATA/SPI H61H2-M5 | |
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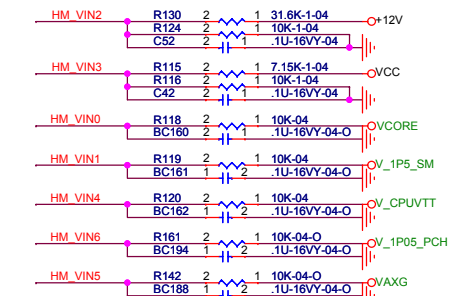
External Connection



HW STRAPPING

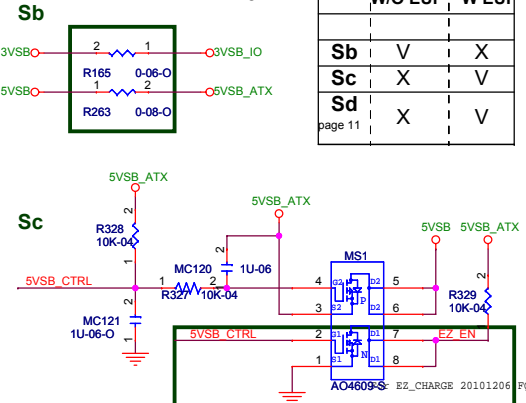


H/W Monitor

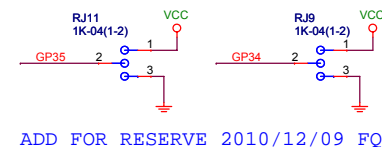


- * HM_VIN0 for VCORE
- * HM_VIN2 for +12V
- * HM_VIN4 for CPUVTT
- * HM_VIN6 for V_1P05_PCH
- * HM_VIN1 for V_DIMM
- * HM_VIN3 for VCC
- * HM_VIN5 for VAXG

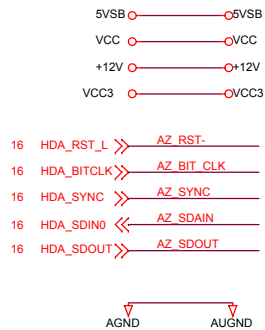
EuP



BIOS SELECTION

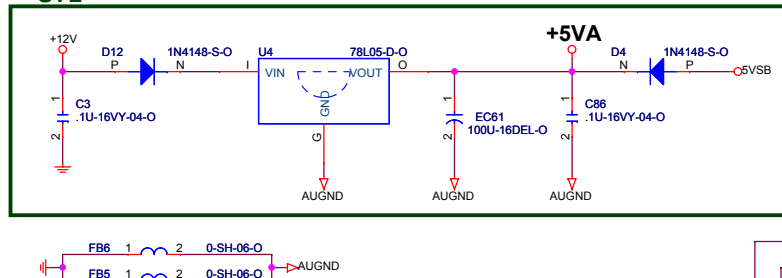


External Connection

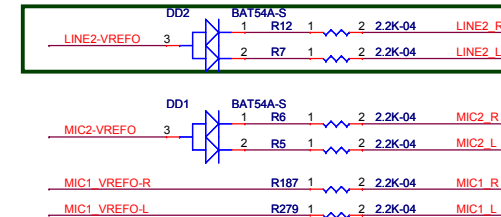


* VCC1.5 can remove for non-Intel G4X platform

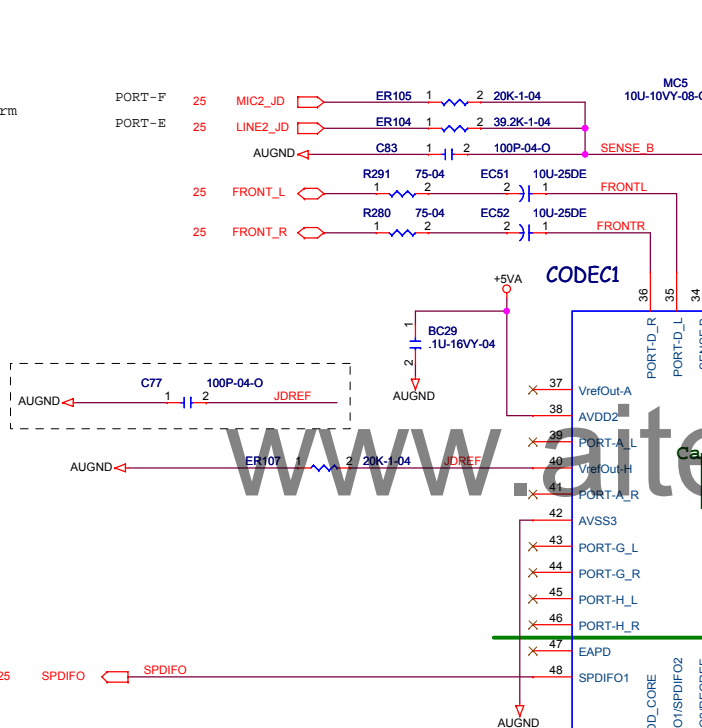
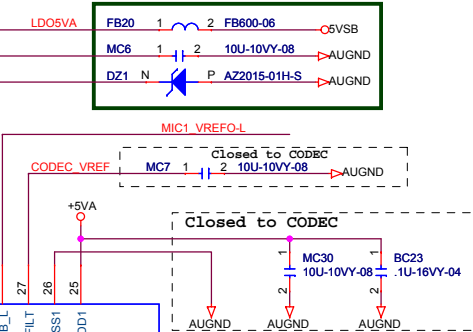
Cv2



Cb



Cv3

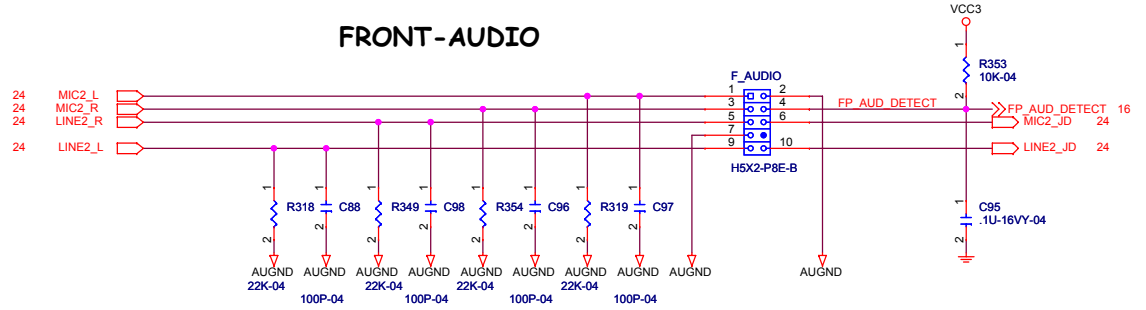
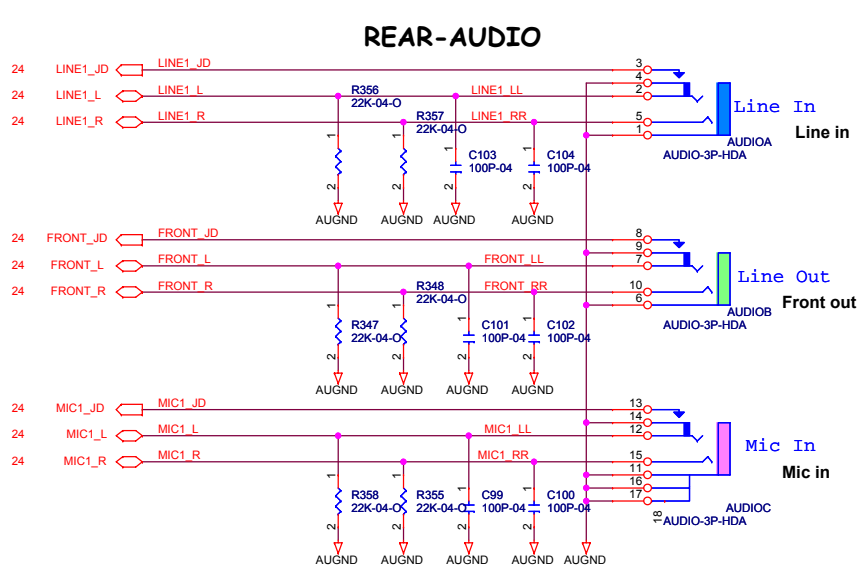


ALC892

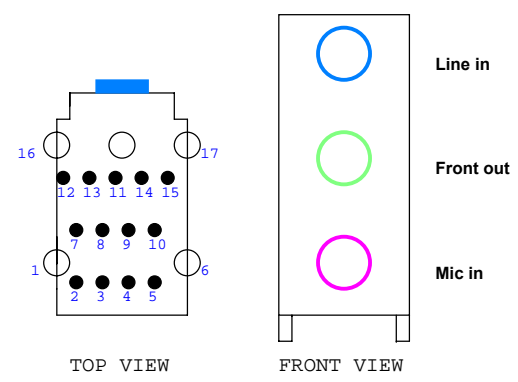
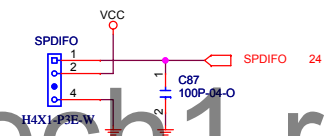
BOM Difference

| Location | ALC892 | ALC662 |
|----------|---------|---------|
| Ca | ALC892 | ALC662 |
| Cb | 2.2K-04 | 3.3K-04 |
| Cv1 | V | X |
| Cv2 | X | V |
| Cv3 | V | X |

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

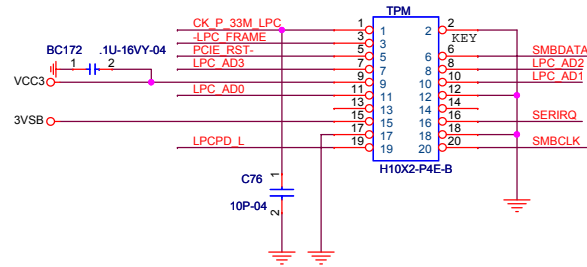
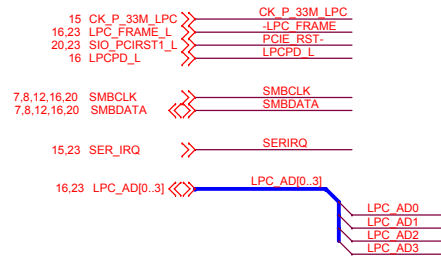


SPDIF-OUT



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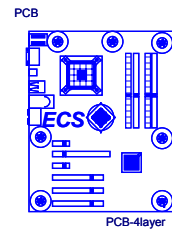
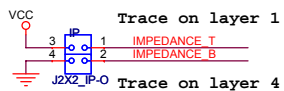
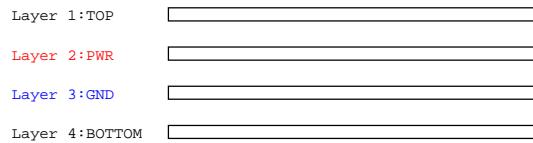
TPM HEADER



DEL LPT HEADER 2010/01/18 FQ

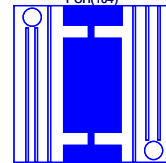
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1)Circuit type 1



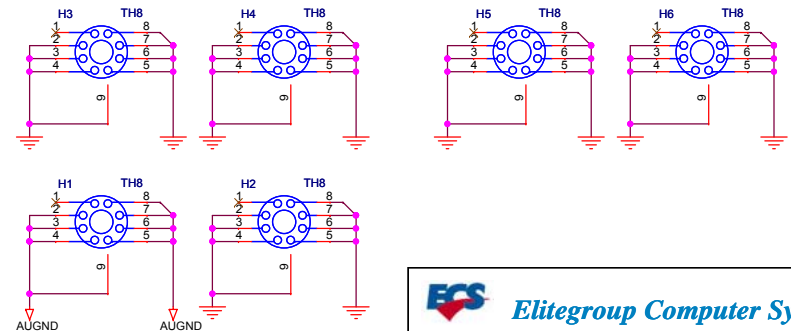
PCB STACK:

- L1:TOP
- L2:PWR
- L3:GND
- L4:BOTTOM



20-120-011476

5series PN:20-120-010851



Elitegroup Computer Systems

Title: **TPM&LPC DEBUG &GND&104**

Size: Custom

Document Number: **H61H2-M5**

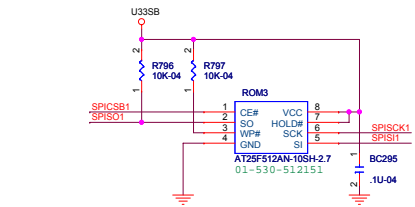
Rev: **2.0**

Date: Tuesday, February 22, 2011

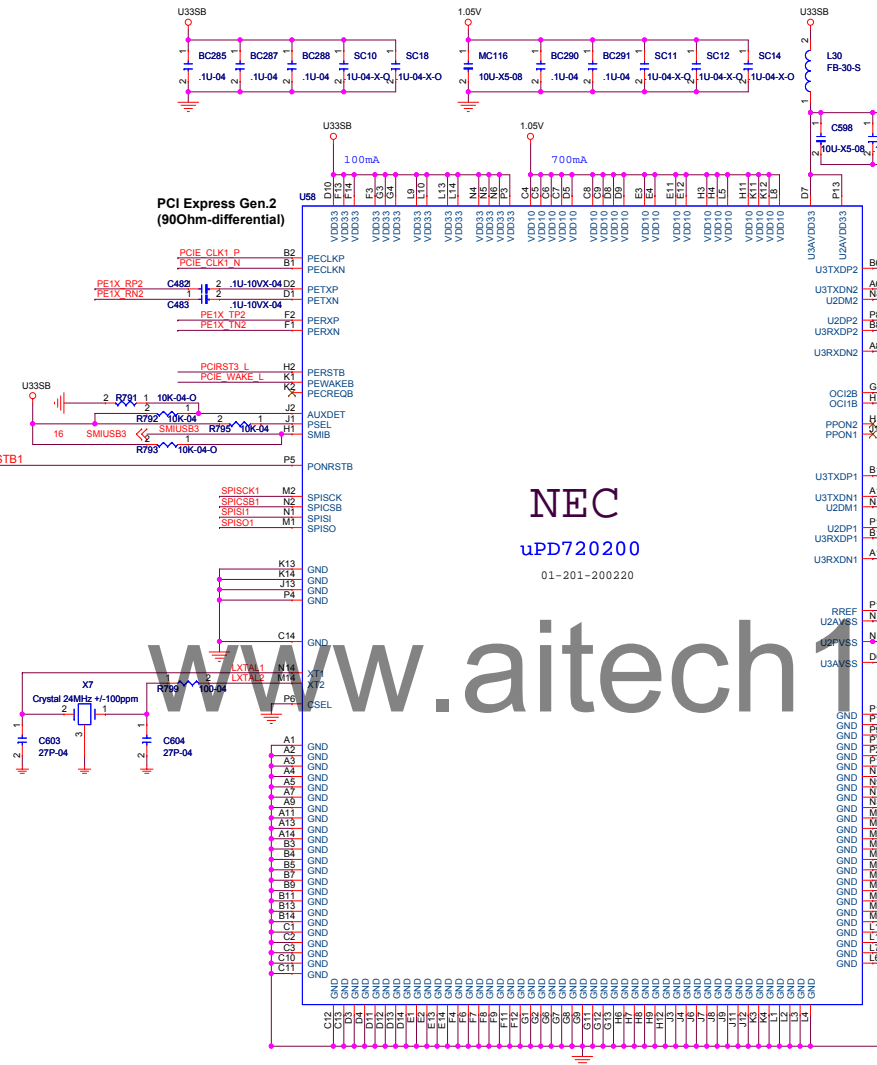
Sheet: 26 of 31

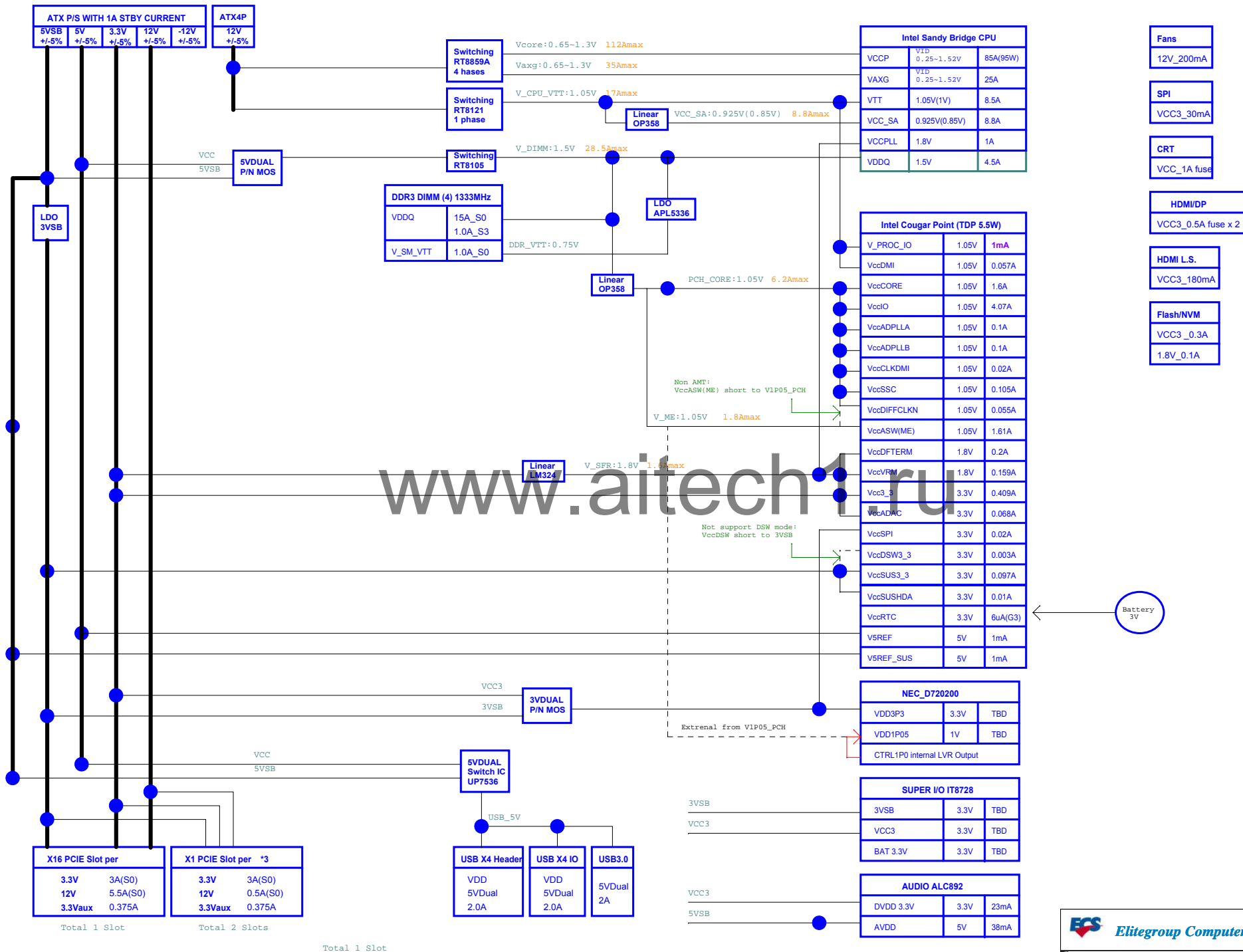
15 CK_PE_USB3_H >> PCIE_CLK1_P
15 CK_PE_USB3_L >> PCIE_CLK1_N
14 USB3_TX_P3 >> PE1X_TP2
14 USB3_TX_N3 >> PE1X_TN2
14 USB3_RX_P3 >> PE1X_RP2
14 USB3_RX_N3 >> PE1X_RN2
4.23.27 SIO_PCIE_RST_L >> PCIRST3_L
16.20.27 PCIE_WAKE_L >> PCIE_WAKE_L

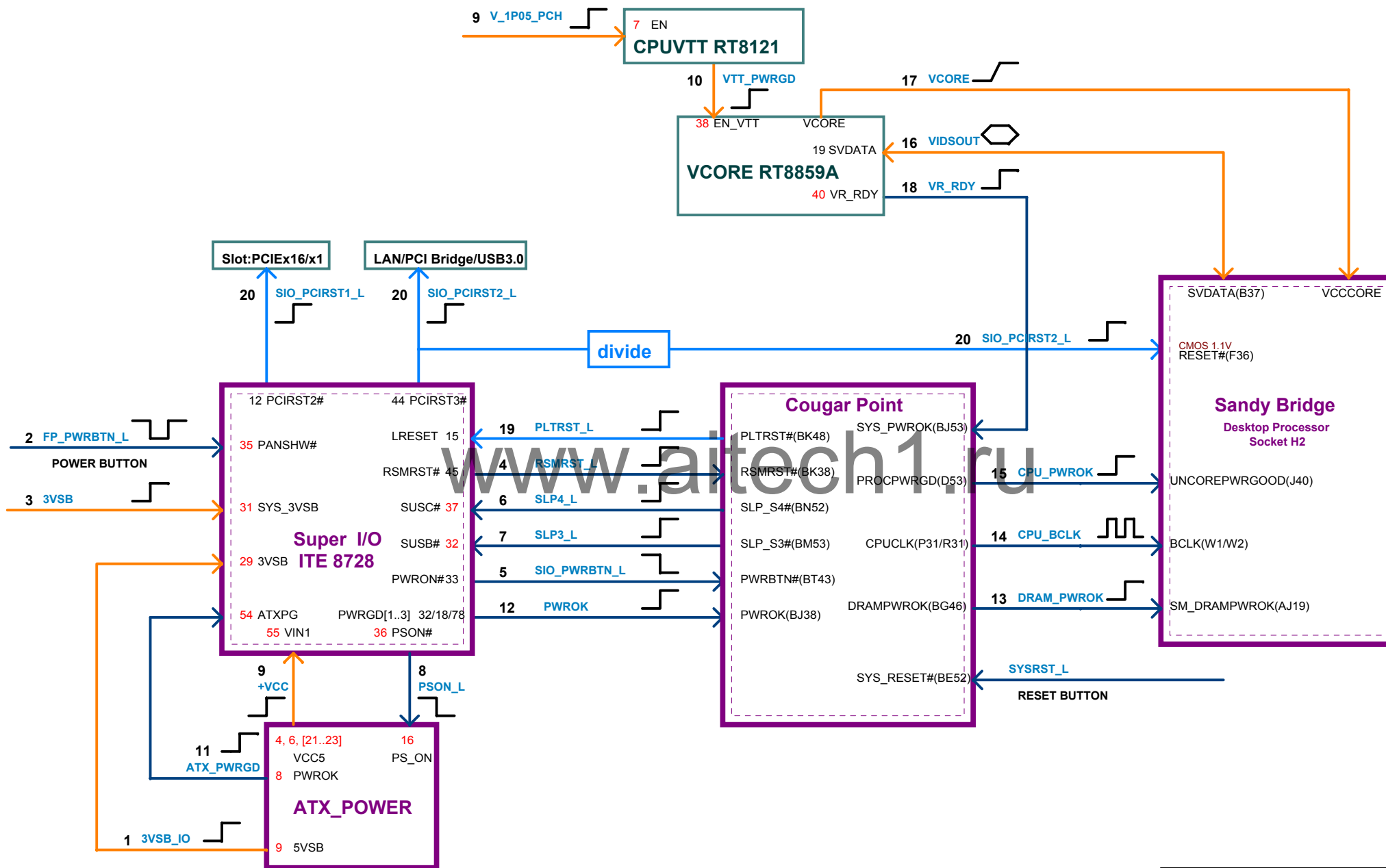
27 U1TP0 >> U1TP0
27 U1TN0 >> U1TN0
27 U1RP0 >> U1RP0
27 U1RN0 >> U1RN0
27 U1TP1 >> U1TP1
27 U1TN1 >> U1TN1
27 U1RP1 >> U1RP1
27 U1RN1 >> U1RN1
27 U2IC_P0 >> U2IC_P0
27 U2IC_N0 >> U2IC_N0
27 U2IC_P1 >> U2IC_P1
27 U2IC_N1 >> U2IC_N1



Note:
1. Every Power trace (3.3V, 1.05V, A3.3V, 12V, 5V, VCCCH1-2) should be broad.
2. 2nd layer of this entire circuit should be grounded.
3. Every high speed signal trace (USB SS/HS, PCI Express), should be wired as shortly as possible.
4. Capacitors C100-113 should be located next to U1, and connected to GND tightly -- by tracing shortly and broadly.
5. For signal traces, routing priority is as follows;
USB SS > PCI Express > (SATA) > USB HS > (DDR) > Ether > PCI, PATA > Other legacy
6. At any crossing for every trace except ground, sufficient area of ground plane between each other should be put.
7. Follow the basic of transmission trace pair when routing any signal trace.
> Remove any impairment or discontinuity.
> Keep same length by each other.
> Keep same width and spacing.
For more information please refer to 'USB3.0 Board Design Guide' in design kit.







NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

